REMARKS

The Final Office Action dated February 10, 2005 has been carefully considered. Claims 1-10 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1 and 5-10 have been amended, and Claim 11 has been cancelled in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

An interview was held with the Examiner, John P. Trimmings, on March 15, 2005, to discuss the rejections under 35 U.S.C. § 103(a) and the proposed amendments thereto. Applicants wish to thank the Examiner for his time and the courtesies extended.

Claims 7 and 10 stand objected to for some informalities. In Claim 7, the phrases "*the* inverted bit" and "*the* second SRL" replace the phrases "an inverted bit" and "a second SRL," respectively. In Claim 10, the language "transmitting the first scan data bit from a *first SRL through a* logic unit to a second SRL" has been added for clarification. Accordingly, Applicants respectfully request that the objections to Claims 7 and 10 be withdrawn and that amended Claims 7 and 10 be allowed.

Claims 6, 7, 10, and 11 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Insofar as these rejections may be applied against the amended claims, they are deemed overcome.

Claim 6 has been amended to describe "transmitting the first scan data bit from the logic unit to the second SRL if there is a logic *0 control* signal," and "transmitting an inverted bit of the first scan data bit from the logic unit to the second SRL if there is *a* logic 1 *control* signal." Furthermore, Claim 6 describes, "receiving a first output data bit of the combinatorial logic by a *last*

SRL *within the SRL chain*, the first output data bit being output from the combinatorial logic receiving at least the first and second scan data bits *in response to a logic 0 control signal*," and "receiving a second output data bit of the combinatorial logic by *the last* SRL *within the SRL chain*, the second output data bit being output from the combinatorial logic receiving at least the inverted bit *from the second SRL* and the second scan data bit *in response to a logic 1 control signal*."

In Claim 7, line 3, the phrase "the inverted bit of" has been deleted for clarity. In addition, the language "the logic 1 *control* signal" replaces the language "the logic 1 signal" in Claims 7, 10, and 11. Accordingly, Applicants respectfully request that the rejections of Claims 7, 10, and 11 under 35 U.S.C. § 112, second paragraph, be withdrawn and that amended Claims 7, 10, and 11 be allowed.

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) in view of U.S. Patent 5,642,362 to Savir ("Savir"), "Scan Latch Design for Delay Test," Jacob Savir, 1997 Test Conference (IEEE Proceedings International), Nov. 1-6 1997, pp 446-453 ("IEEE Proceedings"), and U.S. Patent 6,490,702 to Song ("Song"). Insofar as these rejections may be applied against the amended claims, they are deemed overcome.

Claim 1 has been amended to include a distinguishing feature of the present invention. The last SRL is "*within the SRL chain*" and is "connected to the *output of the* combinatorial logic." Support for this amendment can be found, among other places, in Figure 3 of the original Application.

The Savir, IEEE Proceedings, and Song references do not teach, suggest or disclose this feature of the present invention. Specifically, these cited references do not disclose connecting the output of the combinatorial logic to be tested, to a last SRL within the SRL chain. With this feature the present invention provides many advantages over the cited references. The amount of logic on

the chip is reduced because the testing can be accomplished through the SRL chain, which indicates that no further testing logic is necessary. Furthermore, this invention enhances the flexibility of these tests by using an SRL from the SRL chain. In other words, many different SRLs within the SRL chain can be utilized to test the combinatorial logic. Because of this configuration the present invention provides more flexibility for this type of testing, which enables better performance and lower cost.

In view of the foregoing, it is apparent that the cited references do not disclose, teach, or suggest the unique combination now recited in amended Claim 1. Applicants therefore submit that amended Claim 1 is both clearly and precisely distinguishable over the cited references in a patentable sense, and is therefore allowable over the cited references in any combination. Accordingly, Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 103(a) in view of Savir, IEEE Proceedings, and Song be withdrawn and that amended Claim 1 be allowed.

Claims 2-5 depend upon and further limit amended Claim 1. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejections of dependent Claims 2-5 also be withdrawn.

Claim 6 has been amended to include a distinguishing feature of the present invention. The last SRL is "*within the SRL chain*" and is configured to receive the output of the combinatorial logic. Support for this amendment can be found, among other places, in Figure 3 of the original Application.

The Savir, IEEE Proceedings, and Song references do not teach, suggest or disclose this feature of the present invention. Specifically, these cited references do not disclose connecting the output of the combinatorial logic to be tested, to a last SRL within the SRL chain. With this feature

the present invention provides many advantages over the cited references. The amount of logic on the chip is reduced because the testing can be accomplished through the SRL chain, which indicates that no further testing logic is necessary. Furthermore, this invention enhances the flexibility of these tests by using an SRL from the SRL chain. In other words, many different SRLs within the SRL chain can be utilized to test the combinatorial logic. Because of this configuration of the present invention provides more flexibility for this type of testing, which enables better performance and lower cost.

In view of the foregoing, it is apparent that the cited references do not disclose, teach, or suggest the unique combination now recited in amended Claim 6. Applicants therefore submit that amended Claim 6 is both clearly and precisely distinguishable over the cited references in a patentable sense, and is therefore allowable over the cited references in any combination. Accordingly, Applicants respectfully request that the rejection of Claim 6 under 35 U.S.C. § 103(a) in view of Savir, IEEE Proceedings, and Song be withdrawn and that amended Claim 6 be allowed.

Claims 7-9 depend upon and further limit amended Claim 6. Hence, for at least the aforementioned reasons, these Claims should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejections of dependent Claims 7-9 also be withdrawn.

Claim 10 has been amended to include a distinguishing feature of the present invention. Amended Claim 10 includes the limitations of "*transmitting the first output data bit to a last SRL within the SRL chain*," and "*transmitting the second output data bit to the last SRL within the SRL chain.*" Support for this amendment can be found, among other places, in Figure 3 of the original Application.

The Savir, IEEE Proceedings, and Song references do not teach, suggest or disclose this feature of the present invention. Specifically, these cited references do not disclose connecting the output of the combinatorial logic to be tested, to a last SRL within the SRL chain. With this feature the present invention provides many advantages over the cited references. The amount of logic on the chip is reduced because the testing can be accomplished through the SRL chain, which indicates that no further testing logic is necessary. Furthermore, this invention enhances the flexibility of these tests by using an SRL from the SRL chain. In other words, many different SRLs within the SRL chain can be utilized to test the combinatorial logic. Because of this configuration the present invention provides more flexibility for this type of testing, which enables better performance and lower cost.

In view of the foregoing, it is apparent that the cited references do not disclose, teach, or suggest the unique combination now recited in amended Claim 10. Applicants therefore submit that amended Claim 10 is both clearly and precisely distinguishable over the cited references in a patentable sense, and is therefore allowable over the cited references in any combination. Accordingly, Applicants respectfully request that the rejection of Claim 10 under 35 U.S.C. § 103(a) in view of Savir, IEEE Proceedings, and Song be withdrawn and that amended Claim 10 be allowed.

Claim 11 has been cancelled in this Response. Accordingly, Applicants submit that the rejection of Claim 11 is moot. In addition, the language "*in response to a logic control signal*" has been added to Claim 6 for clarity. The language "*if there is a logic control signal*" has also been added to Claim 10 for clarity.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-10.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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